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EXAMINER	
MATISIAK, JENNIFER E	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/801,205	FARNWORTH ET AL.	
	Examiner	Art Unit	
	Jennifer Matisiak	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-84 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-84 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 16 March 2004 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 03102006.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 1, 22 and 64 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding claims 1, 22 and 64, the claim limitation: "a semiconductor die having at least one circuit comprising: a semiconductor die having at least one circuit" is confusing language. Claims are rendered indefinite since it is unclear whether applicant's invention comprises two separate die or the claim limitation is redundant.

Drawings

2. The drawings are objected to because regarding Fig. 6, the solder ball and one resilient connector shown are misnumbered; they appear to have been switched. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and

where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d): If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 11, 15, 22, 32, 34, 36, 40, 41, 42, 43, 57, 61, 62, 63, 64, 74, 76, 78, 82, 83 and 84 are rejected under 35 U.S.C. 102(a) as being anticipated by Doan et al. (US 2005/0167798), hereinafter Doan.

Regarding claim 1, Doan discloses a semiconductor die (Fig. 3A, for example) having at least one circuit connected to at least one component (para [0033]) comprising: a semiconductor die having an active surface (144), an inactive surface (152) and at least one circuit (para [0039]): at least one bond pad (142 of Fig. 3B)

formed on a portion of the active surface; and at least one bond pad (150) formed on a portion of the inactive surface of the semiconductor die. Doan discloses a device wherein at least one bond pad formed on a portion of the inactive surface of the semiconductor die is capable of being used for protecting a portion of the semiconductor die. Additionally, the limitation "for protecting a portion of the semiconductor die" is considered to be functional language.

> While features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. *In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997) (The absence of a disclosure in a prior art reference relating to function did not defeat the Board's finding of anticipation of claimed apparatus because the limitations at issue were found to be inherent in the prior art reference); see also *In re Swinehart*, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971); *In re Danly,* 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). "[A]pparatus claims cover what a device *is*, not what a device *does*." *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) (emphasis in original).

Regarding claim 11, Doan discloses a semiconductor die (Fig. 3A) further comprising: at least one resilient connector (148, para [0039]) attached to a portion of the active surface (144) of the semiconductor die and a portion of a surface of a substrate (para [0015]).

Regarding claim 15, Doan discloses a semiconductor die (Fig. 3B) wherein the semiconductor die includes at least a portion of one metal protection layer (146) located on a portion of the active surface (144) of the semiconductor die.

Regarding claim 19, Doan discloses a semiconductor die (Fig. 3B) wherein the semiconductor die includes a portion of at least one metal protection layer (146) having a portion thereof located adjacent an edge of the semiconductor die.

Regarding claim 22, Doan discloses a semiconductor die (Fig. 3A) having at least one circuit connected to at least one component (para [0033]) and a substrate (para [0015]) comprising: a semiconductor die having an active surface (144), an inactive surface (152) and at least one circuit (para [0039]), the semiconductor die including at least one bond pad (112 of Fig. 2A) formed on a portion of the active surface thereof connected to the at least one circuit and at least one bond pad (150) formed on a portion of the inactive surface; and a substrate (para [0015]) having a portion thereof connected to the at least one bond pad formed on the portion of the active surface of the semiconductor die (para [0040]).

Doan discloses a device wherein at least one bond pad formed on a portion of the inactive surface of the semiconductor die is capable of being used for protecting a portion of the semiconductor die. Additionally, the limitation "for protecting a portion of the semiconductor die" is considered to be functional language, as discussed above.

Regarding claim 32, Doan discloses a semiconductor die (Fig. 3A) and substrate (para [0015]) further comprising: at least one resilient connector (148, para [0039]) attached to a portion of the active surface (144) of the semiconductor die and a portion of a surface of the substrate (para [0015]).

Regarding claim 34, Doan discloses a semiconductor die (Fig. 3A) and substrate (para [0015]) wherein the at least one resilient connector (148, para [0039]) includes a circular shape.

Regarding claim 36, Doan discloses a semiconductor die (Fig. 3B) and substrate (para [0015]) wherein the semiconductor die includes at least a portion of one metal protection layer (146) located on a portion of the active surface of the semiconductor die.

Regarding claim 40, Doan discloses a semiconductor die (Fig. 3B) and substrate (para [0015]) wherein the semiconductor die includes a portion of at least one metal protection layer (146) having a portion thereof located adjacent an edge of the semiconductor die.

Regarding claim 41, Doan discloses a semiconductor die (Fig. 3A) and substrate (para [0015]). Doan does not explicitly state "wherein the semiconductor die includes at least one trace extending from at least a portion of the at least one bond pad formed on the portion of the active surface of the semiconductor die." However, it is inherent that a trace extends from at least a portion of the at least one bond pad (112 of Fig. 2A) formed on the portion of the active surface (144 of Fig. 3A) of the semiconductor die since such a trace is necessary to operate the input/output terminals of the device of Doan.

Regarding claim 42, Doan discloses a semiconductor die (Fig. 3A) and substrate (para [0015]) further comprising at least one connector (148, para [0039]) located on a portion of the at least one trace.

Regarding claim 43, Doan discloses a method comprising: forming an area of metal (150) on a surface of the semiconductor die (Fig. 3A).

Doan discloses a method wherein formed an area of metal on a surface of the semiconductor die is capable of being used for protecting a portion of the semiconductor die. Additionally, the limitations "of relieving forces on a semiconductor die... for protecting a portion of the semiconductor die" is considered to be functional language, as discussed above.

Regarding claim 57, Doan discloses a method (para [0040]) wherein the semiconductor die (Fig. 3B) includes at least a portion of one metal protection layer (146) located on a portion of an active surface (144) thereof.

Regarding claim 61, Doan discloses a method (para [0040]), wherein the semiconductor die (Fig. 3B) includes a portion of at least one metal protection layer (146) located adjacent an edge of the semiconductor die.

Regarding claim 62, Doan discloses a method (para [0040]). Doan does not explicitly state "wherein the semiconductor die includes at least one trace extending from at least a portion of the area of metal formed on the surface of the semiconductor die." However, it is inherent that a trace extends from at least a portion of the area of metal (112 of Fig. 2A) formed on the portion of the active surface (144) of the semiconductor die (Fig. 3A) since such a trace is necessary to operate the input/output terminals of the device of Doan.

Regarding claim 63, Doan discloses a method (para [0040]) further comprising at least one connector (148 of Fig. 3B). Doan does not explicitly state "located on a portion

of the at least one trace." However, it is inherent that at least one connector is located on a portion of the at least one trace since such a trace is necessary to operate the input/output terminals of the device of Doan.

Regarding claim 64, Doan discloses a method (para [0040]) of forming a semiconductor die (Fig. 3A) having at least one circuit connected to at least one component (para [0039]) and a substrate (para [0015]) comprising: providing a semiconductor die having an active surface (144) and an inactive surface (152), the semiconductor die including at one bond pad (112 of Fig. 2A) formed on a portion of the active surface connected to one circuit and one bond pad (150) formed on a portion of the inactive surface; and attaching a substrate (para [0015]) having a portion thereof connected to one bond pad formed on the portion of the active surface of the semiconductor die.

Doan discloses a method wherein formed an area of metal on a surface of the semiconductor die is capable of being used for protecting a portion of the semiconductor die. Additionally, the limitation "of relieving forces on a semiconductor die... for protecting a portion of the semiconductor die" is considered to be functional language, as discussed above.

Regarding claim 74, Doan discloses a method (para [0040]) further comprising: attaching at least one resilient connector (148 of Fig. 3A, para [0039]) to a portion of the active surface (144) of the semiconductor die and a portion of a surface of the substrate (para [0015]).

Regarding claim 76, Doan discloses a method (para [0040]), wherein the at least one resilient connector (148 of Fig. 3A, para [0039]) includes a circular shape.

Regarding claim 78, Doan discloses a method (para [0040]) wherein the semiconductor die (Fig. 3B) includes at least a portion of one metal protection layer (146) located on a portion of the active surface (144) thereof.

Regarding claim 82, Doan discloses a method (para [0040]) wherein the semiconductor die (Fig. 3B) includes a portion of at least one metal protection layer (146) located adjacent an edge thereof.

Regarding claim 83, Doan discloses a method (para [0040]). Doan does not explicitly state "wherein the semiconductor die includes at least one trace extending from at least a portion of the area of metal formed on the surface of the semiconductor die." However, it is inherent that a trace extends from at least a portion of the area of metal (112 of Fig. 2A) formed on the portion of the active surface (144) of the semiconductor die (Fig. 3A) since such a trace is necessary to operate the input/output terminals of the device of Doan.

Regarding claim 84, Doan discloses a method (para [0040]) further comprising at least one connector (148 of Fig. 3A, para [0039]). Doan does not explicitly state "located on a portion of the at least one trace." However, it is inherent that a connector is located on a portion of the at least one trace since such a trace is necessary to provide electrical connection from the connector to the die of the device of Doan.

4. Claims 1-2, 5-9, 12, 20-23, 26-30, 33, 41, 44, 46, 49-53, 55, 62, 64-65, 68-72 and 75 are rejected under 35 U.S.C. 102(b) as being anticipated by Fang et al. (US 2003/0127717), hereinafter Fang.

Regarding claim 1, Fang discloses a semiconductor die (312 of Fig. 3, for example) having at least one circuit connected to at least one component comprising: a semiconductor die (312) having an active surface (para [0016]), an inactive surface (para [0016]) and at least one circuit: at least one bond pad (para [0005]) formed on a portion of the active surface; and at least one bond pad (3121) formed on a portion of the inactive surface of the semiconductor die.

Fang discloses a device wherein at least one bond pad formed on a portion of the inactive surface of the semiconductor die is capable of being used for protecting a portion of the semiconductor die. Additionally, the limitation "for protecting a portion of the semiconductor die" is considered to be functional language.

> While features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. *In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997) (The absence of a disclosure in a prior art reference relating to function did not defeat the Board's finding of anticipation of claimed apparatus because the limitations at issue were found to be inherent in the prior art reference); see also *In re Swinehart*, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971); *In re Danly,* 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). "[A]pparatus claims cover what a device *is*, not what a device *does*." *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) (emphasis in original).

Regarding claim 2, Fang discloses a semiconductor die (Fig. 3) wherein the at least one bond pad (3121) formed on the portion of the inactive surface (para [0016]) of the semiconductor die (312) includes a bond pad connected to the at least one circuit of the semiconductor die (para [0016]).

Regarding claim 5, Fang discloses a semiconductor die (Fig. 3) further comprising: a substrate (35) having a portion thereof connected to the at least one bond pad (para [0005]) formed on the portion of the active surface (para [0016]) of the semiconductor die (312), the substrate having at least one circuit connected to the at least one bond pad formed on the active surface of the semiconductor die; and at least one bond wire (33) connected to the at least one pad (3121) formed on the portion of the inactive surface (para [0016]) of the semiconductor die.

Regarding claim 6, Fang discloses a semiconductor die (Fig. 3) wherein the substrate (35) includes a portion thereof located adjacent at least one edge of the semiconductor die (312).

Regarding claim 7, Fang discloses a semiconductor die (Fig. 3) further comprising a sealant material (36) located between a portion of the semiconductor die (312) and a portion of the substrate (35).

Regarding claim 8, Fang discloses a semiconductor die (Fig. 3) further comprising a sealant material (36) located along a portion of at least one edge of the semiconductor die (312) and a portion of the substrate (35).

Regarding claim 9, Fang discloses a semiconductor die (Fig. 3) wherein a bond pad (para [0005]) formed on the portion of the active surface (para [0016]) is connected to a contact pad (39) on a portion of a surface of the substrate (35).

Regarding claim 12, Fang discloses a semiconductor die (Fig. 3) wherein one bond pad (3121) formed on the portion of the inactive surface (para [0016]) of the semiconductor die includes a rectangular shape (3121c of Fig. 4).

Regarding claim 20, Fang discloses a semiconductor die (Fig. 3). Fang does not explicitly state "wherein the semiconductor die includes at least one trace extending from at least a portion of the at least one bond pad formed on the portion of the active surface of the semiconductor die." However, it is inherent that a trace extends from at least a portion of the at least one bond pad (para [0005]) formed on the portion of the active surface (para [0016]) of the semiconductor die since such a trace is necessary to operate the input/output terminals of the device of Fang.

Regarding claim 21, Fang discloses a semiconductor die (Fig. 3) further comprising at least one connector (3122) located on a portion of the at least one trace. However, it is inherent that at least one connector is located on a portion of the at least one trace of the semiconductor die since such a trace is necessary to operate the input/output terminals of the device of Fang.

Regarding claim 22, Fang discloses a semiconductor die (Fig. 3) having at least one circuit connected to at least one component and a substrate (35) comprising: a semiconductor die having an active surface (para [0016]), an inactive surface (para [0016]) and at least one circuit, the semiconductor die (312) including at least one bond

pad (para [0005]) formed on a portion of the active surface (para [0016]) thereof connected to the at least one circuit and at least one bond pad (3121) formed on a portion of the inactive surface (para [0016]); and a substrate (35) having a portion thereof connected to the at least one bond pad formed on the portion of the active surface of the semiconductor die.

Fang discloses a device wherein at least one bond pad formed on a portion of the inactive surface of the semiconductor die is capable of being used for protecting a portion of the semiconductor die. Additionally, the limitation "for protecting a portion of the semiconductor die" is considered to be functional language, as discussed above.

Regarding claim 23, Fang discloses a semiconductor die (312 of Fig. 3) and substrate (35) wherein one bond pad (3121) formed on the portion of the inactive surface (para [0016]) of the semiconductor die includes a bond pad connected to the at least one circuit of the semiconductor die.

Regarding claim 26, Fang discloses a semiconductor die (312 of Fig. 3) and substrate (35) further comprising: at least one bond wire (32) connected to the at least one bond pad (3121) formed on the portion of the inactive surface (para [0016]) of the semiconductor die.

Regarding claim 27, Fang discloses a semiconductor die (312 of Fig. 3) and substrate (35) wherein the substrate includes a portion thereof located adjacent at least one edge of the semiconductor die.

Regarding claim 28, Fang discloses a semiconductor die (312 of Fig. 3) and substrate (35) further comprising a sealant material (36) located between a portion of the semiconductor die and a portion of the substrate.

Regarding claim 29, Fang discloses a semiconductor die (312 of Fig. 3) and substrate (35) further comprising a sealant material (36) located along a portion of at least one edge of the semiconductor die and a portion of the substrate.

Regarding claim 30, Fang discloses a semiconductor die (312 of Fig. 3) and substrate (35) wherein one bond pad (para [0005]) formed on the portion of the active surface (para [0016]) is connected to a contact pad (39) on a portion of a surface of the substrate.

Regarding claim 33, a semiconductor die (312 of Fig. 3) and substrate (35) wherein one bond pad (3121) formed on the portion of the inactive surface (para [0016]) of the semiconductor die includes a rectangular shape (3121c of Fig. 4).

Regarding claim 41, Fang discloses a semiconductor die (312 of Fig. 3) and substrate (35). While Fang does not explicitly state "wherein the semiconductor die includes at least one trace extending from at least a portion of the at least one bond pad formed on the portion of the active surface of the semiconductor die." It is inherent that a trace extends from at least a portion of the at least one bond pad (para [0005]) formed on the portion of the active surface (para [0016]) of the semiconductor die since such a trace is necessary to operate the input/output terminals of the device of Fang.

Regarding claim 43, Fang discloses a method (para [0016]) comprising: forming an area of metal (para [0005]) on a surface of the semiconductor die (312 of Fig. 3).

Fang discloses a method wherein formed an area of metal on a surface of the semiconductor die is capable of being used for protecting a portion of the semiconductor die. Additionally, the limitations "of relieving forces on a semiconductor die...for protecting a portion of the semiconductor die" is considered to be functional language, as discussed above.

Regarding claim 44, Fang discloses a method (para [0016]) further comprising; providing a substrate (35 of Fig. 3); connecting the area of metal (para [0005]) to a portion of the substrate. Fang does not explicitly state "and applying a force between the substrate and the area of metal." However, it is inherent that force must be applied between the substrate and the area of metal since the bumps to which area of metal is connected is welded to the substrate (para [0005]).

Regarding claim 46, Fang discloses a method (para [0016]) wherein the area of metal comprises one bond pad (3121 of Fig. 3) formed on a portion of an inactive surface (para [0016]) of the semiconductor die connected to a circuit of the semiconductor die.

Regarding claim 49, Fang discloses a method (para [0016]) further comprising: forming a substrate (35 of Fig. 3) having a portion thereof connected to one bond pad (3121) formed on a portion of the inactive surface (para [0016]) of the semiconductor die (312), the substrate having at least one circuit connected to the at least one bond pad of the semiconductor die; and at least one bond wire (32) connected to the at least one bond pad formed on the inactive surface of the semiconductor die.

Regarding claim 50, Fang discloses a method (para [0016]) wherein the substrate (35 of Fig. 3) includes a portion thereof located adjacent at least one edge of the semiconductor die.

Regarding claim 51, Fang discloses a method (para [0016]) further comprising applying a sealant material (36 of Fig. 3) located between a portion of the semiconductor die and a portion of the substrate (35).

Regarding claim 52, Fang discloses a method (para [0016]) further comprising applying a sealant material (36 of Fig. 3) located along a portion of at least one edge of the semiconductor die and a portion of the substrate.

Regarding claim 53, Fang discloses a method (para [0016]) further comprising: connecting one bond pad (3121 of Fig. 3) formed on the inactive surface (para [0016]) to a contact pad (39) on a portion of a surface of the substrate (35).

Regarding claim 55, Fang discloses a method (para [0016]) wherein one bond pad (3121 of Fig. 3) formed on the inactive surface (para [0016]) of the semiconductor die (312) includes a rectangular shape (3121c of Fig. 4).

Regarding claim 62, Fang discloses a method (para [0016]). Fang does not explicitly state "wherein the semiconductor die includes at least one trace extending from at least a portion of the area of metal formed on the surface of the semiconductor die." However, it is inherent that a trace extends from at least a portion of at least a portion of the area of metal (para [0005]) formed on the surface (para [0016]) of the semiconductor die (312 of Fig. 3) since such a trace is necessary to operate the input/output terminals of the device of Fang.

Regarding claim 64, Fang discloses a method (para [0016]) of forming a semiconductor die (312 of Fig. 3) having at least one circuit connected to at least one component and a substrate (35) comprising: providing a semiconductor die having an active surface and an inactive surface (para [0016]), the semiconductor die including at least one bond pad (para [0005]) formed on a portion of the active surface connected to one circuit and one bond pad (3121) formed on a portion of the inactive surface; and attaching a substrate (35) having a portion thereof connected to one bond pad formed on the portion of the active surface of the semiconductor die.

Fang discloses a method wherein at least one bond pad formed on a portion of the inactive surface of the die is capable of being used for protecting a portion of the semiconductor die. Additionally, the limitation "of relieving forces on a semiconductor die " is considered to be functional language, as discussed above.

Regarding claim 65, Fang discloses a method (para [0016]) wherein one bond pad (3121 of Fig. 3) formed on the portion of the inactive surface (para [0016]) of the semiconductor die includes a bond pad (para [0005]) connected to a circuit of the semiconductor die (312).

Regarding claim 68, Fang discloses a method (para [0016]) further comprising: connecting one bond wire (32 of Fig. 3) to the at least one bond pad (3121) formed on the inactive surface (para [0016]) of the semiconductor die (312).

Regarding claim 69, Fang discloses a method (para [0016]) wherein the substrate (35 of Fig. 3) includes a portion thereof located adjacent at least one edge of the semiconductor die (312).

Regarding claim 70, Fang discloses a method (para [0016]) further comprising applying a sealant material (36 of Fig. 3) located between a portion of the semiconductor die (312) and a portion of the substrate (35).

Regarding claim 71, Fang discloses a method (para [0016]) further comprising applying a sealant material (36 of Fig. 3) located along a portion of at least one edge of the semiconductor die (312) and a portion of the substrate (35).

Regarding claim 72, Fang discloses a method (para [0016]) further comprising: connecting the one bond pad (para [0005]) formed on the portion of the active surface (para [0016]) of the semiconductor die (312 of Fig. 3) to a contact pad (39) on a portion of a surface of the substrate (35).

Regarding claim 75, Fang discloses a method (para [0016]) wherein one bond pad (3121 of Fig. 3) formed on the inactive surface (para [0016]) of the semiconductor die (312) includes a rectangular shape (3121c of Fig. 4).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 10, 13, 14, 31, 35, 54, 56 and 77 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fang as applied to claims 1, 22, 43 and 64 above, and further in view of Doan.

Regarding claim 10, Fang discloses the limitations of claim 5. Fang does not disclose "a semiconductor die further comprising: at least one resilient connector attached to a portion of the active surface of the semiconductor die and a portion of a surface of the substrate." Doan discloses a semiconductor die (Fig. 3A) further comprising: at least one resilient connector (148) attached to a portion of the active surface (144) of the semiconductor die and a portion of a surface of the substrate (para [0015]). It would have been obvious to one of ordinary skill in the art to include resilient connectors in the invention of Fang since the bumps of the invention of Fang may comprise any material including the material which comprises resilient connectors as disclosed by applicant.

Regarding claim 13, Fang and Doan disclose the limitations of claim 10. Furthermore Fang discloses a semiconductor die (Fig. 3) wherein the at least one bump includes a circular shape. If the proposed modification had been made to the invention of Fang, the resilient connections would have a circular shape.

Regarding claim 14, Fang discloses the limitations of claim 5. Fang does not disclose "wherein the substrate includes at least one resilient connector located on a surface thereon abutting a portion of the semiconductor die." Doan discloses a die (Fig. 3A) wherein the substrate (para [0015]) includes at least one resilient connector (148, para [0039]) located on a surface thereon abutting a portion of the semiconductor die. It

would have been obvious to one of ordinary skill in the art to include resilient connectors abutting a portion of the semiconductor die in the invention of Fang since the bumps of the invention of Fang may comprise any material including the material for the resilient connectors as disclosed by the applicant. Moreover, Fang discloses bumps (3122 of Fig. 3) abutting a portion of the semiconductor die as shown above.

Regarding claim 31, Fang discloses the limitations of claim 26. Fang does not disclose "a semiconductor die further comprising: at least one resilient connector attached to a portion of the active surface of the semiconductor die and a portion of a surface of the substrate." Doan discloses a semiconductor die (Fig. 3A) further comprising: at least one resilient connector (148) attached to a portion of the active surface (144) of the semiconductor die and a portion of a surface of the substrate (para [0015]). It would have been obvious to one of ordinary skill in the art to include resilient connectors in the invention of Fang since the bumps of the invention of Fang may comprise any material including the material which comprises resilient connectors as disclosed by applicant.

Regarding claim 35, Fang discloses the limitations of claim 26. Fang does not disclose "wherein the substrate includes at least one resilient connector located on a surface thereon abutting a portion of the semiconductor die." Doan discloses a die (Fig. 3A) wherein the substrate (para [0015]) includes at least one resilient connector (148, para [0039]) located on a surface thereon abutting a portion of the semiconductor die. It would have been obvious to one of ordinary skill in the art to attach resilient connectors abutting a portion of the semiconductor die in the invention of Fang since the bumps of

the invention of Fang may comprise any material including the material for the resilient connectors as disclosed by the applicant. Moreover, Fang discloses bumps (3122 of Fig. 3) abutting a portion of the semiconductor die as shown above.

Regarding claim 54, Fang discloses the limitations of claim 49. Fang does not disclose "a method further comprising: attaching at least one resilient connector to a portion of the active surface of the semiconductor die and a portion of a surface of the substrate." Doan discloses a method (para [0040]) further comprising: attaching at least one resilient connector (148 of Fig. 3A) to a portion of the active surface (144) of the semiconductor die and a portion of a surface of the substrate (para [0015]). It would have been obvious to one of ordinary skill in the art to attach resilient connectors in the invention of Fang since the bumps of the invention of Fang may comprise any material including the material which comprises resilient connectors as disclosed by applicant.

Regarding claim 56, Fang discloses the limitations of claim 49. Fang does not disclose "wherein the substrate includes at least one resilient connector located on a surface thereon abutting a portion of the semiconductor die." Doan discloses a method (para [0040]) wherein the substrate (para [0015]) includes at least one resilient connector (148, para [0039]) located on a surface thereon abutting a portion of the semiconductor die. It would have been obvious to one of ordinary skill in the art to include resilient connectors abutting a portion of the semiconductor die in the invention of Fang since the bumps of the invention of Fang may comprise any material including the material for the resilient connectors as disclosed by the applicant. Moreover, Fang

discloses bumps (3122 of Fig. 3) abutting a portion of the semiconductor die as shown above.

Regarding claim 77, Fang discloses the limitations of claim 68. Fang does not disclose "wherein the substrate includes at least one resilient connector located on a surface thereon abutting a portion of the semiconductor die." Doan discloses a method (para [0040]) wherein the substrate (para [0015]) includes at least one resilient connector (148, para [0039]) located on a surface thereon abutting a portion of the semiconductor die. It would have been obvious to one of ordinary skill in the art to include resilient connectors abutting a portion of the semiconductor die in the invention of Fang since the bumps of the invention of Fang may comprise any material including the material for the resilient connectors as disclosed by the applicant. Moreover, Fang discloses bumps (3122 of Fig. 3) abutting a portion of the semiconductor die as shown above.

6. Claims 3-4, 24-25, 47-48 and 66-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fang as applied to claims 1, 22, 43 and 64 above, and further in view of Chu et al. (US 20040099961), hereinafter Chu.

Regarding claim 3, Fang discloses the limitations of claim 1. Fang does not disclose "wherein the at least one bond pad formed on the portion of the inactive surface includes a bond pad having more than one layer of material." Chu discloses (Fig. 6B, for example) a bond pad (35) having more than one layer of material (35c, para [0032]). It would have been obvious to one of ordinary skill in the art at the time the

invention was made to include bond pads of more than one layer in the invention of Fang in order to prevent oxidation of the bond pads.

Regarding claim 4, Fang and Chu disclose the limitations of claim 3. Moreover, Chu discloses a bond pad having more than one layer of material, each layer of material comprising a different metal (para [0032]). It is inherent that the different metal materials, specifically copper and gold, have different coefficients of thermal expansion.

Regarding claim 24, Fang discloses the limitations of claim 22. Fang does not disclose "wherein the at least one bond pad formed on the portion of the inactive surface includes a bond pad having more than one layer of material." Chu discloses (Fig. 6B, for example) a bond pad (35) having more than one layer of material (35c, para [0032]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include bond pads of more than one layer in the invention of Fang in order to prevent oxidation of the bond pads.

Regarding claim 25, Fang and Chu disclose the limitations of claim 24. Moreover, Chu discloses a bond pad having more than one layer of material, each layer of material comprising a different metal (para [0032]). It is inherent that the different metal materials, specifically copper and gold, have different coefficients of thermal expansion.

Regarding claim 47, Fang discloses the limitations of claim 46. Fang does not disclose "wherein the at least one bond pad formed on a portion of the inactive surface includes a bond pad having more than one layer of material." Chu discloses (Fig. 6B, for example) a bond pad (35) having more than one layer of material (35c, para [0032]). It would have been obvious to one of ordinary skill in the art at the time the invention was

made to include bond pads of more than one layer in the invention of Fang in order to prevent oxidation of the bond pads.

Regarding claim 48, Fang and Chu disclose the limitations of claim 47. Moreover, Chu discloses a bond pad having more than one layer of material, each layer of material comprising a different metal (para [0032]). It is inherent that the different metal materials, specifically copper and gold, have different coefficients of thermal expansion.

Regarding claim 66, Fang discloses the method of claim 64. Fang does not disclose "wherein the at least one bond pad formed on the portion of the inactive surface includes a bond pad having more than one layer of material." Chu discloses (Fig. 6B, for example) a bond pad (35) having more than one layer of material (35c, para [0032]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include bond pads of more than one layer in the invention of Fang in order to prevent oxidation of the bond pads.

Regarding claim 67, Fang and Chu disclose the method of claim 66. Moreover, Chu discloses a bond pad having more than one layer of material, each layer of material comprising a different metal (para [0032]). It is inherent that the different metal materials, specifically copper and gold, have different coefficients of thermal expansion.

7. Claims 66 and 73 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doan as applied to claim 64 above, and further in view of Chu.

Regarding claim 66, Doan discloses the method of claim 64. Doan does not disclose "wherein the at least one bond pad formed on the portion of the inactive

surface includes a bond pad having more than one layer of material." Chu discloses (Fig. 6B, for example) a bond pad (35) having more than one layer of material (35c, para [0032]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include bond pads of more than one layer in the invention of Doan in order to prevent oxidation of the bond pads.

Regarding claim 73, Doan and Chu disclose the method of claim 66. Moreover, Doan discloses attaching at least one resilient connector (148, para [0039]) to a portion of the active surface (144) of the semiconductor die (Fig. 3A) and a portion of a surface of the substrate (para [0015]).

8. Claims 16-18, 37-39, 45, 58-60 and 79-81 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doan as applied to claims 1, 22, 43 and 64 above, and further in view of Kuo et al. (US 20050121804), hereinafter Kuo.

Regarding claim 16, Doan discloses the limitations of claim 1. Doan does not disclose "wherein the semiconductor die includes a first passivation layer located on a portion thereof and a second passivation layer located on a portion of the first passivation layer." Kuo discloses a semiconductor die (100 of Fig. 1F, for example) which includes a first passivation layer (192c) located on a portion thereof and a second passivation layer (192d) located on a portion of the first passivation layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a second passivation layer located on a portion of a first passivation layer

located on the die of the invention of Doan since it is desirable to eliminate moisture and static charge build up due to ambient interference.

Regarding claim 17, Doan discloses the limitations of claim 1, wherein the semiconductor die (Fig. 3A) includes at least a portion of one metal protection layer (146) located on a portion of the active surface of the semiconductor die. Doan does not disclose "a first passivation layer located on a portion of the one metal protection layer, and a second passivation layer located on a portion of the first passivation layer."

Kuo discloses a semiconductor die (100 of Fig. 1F) which includes a first passivation (192c) layer located on a portion of the one metal protection layer (150b, para [0028]), and a second passivation layer (192d) located on a portion of the first passivation layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a second passivation layer located on a portion of a first passivation layer located on a metal protection layer located on a die in the invention of Doan since it is desirable to eliminate moisture and static charge build up due to ambient interference.

Regarding claim 18, Doan discloses the limitations of claim 1. Doan does not disclose "wherein the semiconductor die includes at least a portion of more than one metal protection layer located on a portion of the active surface of the semiconductor die, a first passivation layer located on a portion on the metal protection layer, and a plurality of passivation layers located on at least a portion of the first passivation layer." Kuo discloses semiconductor die (100 of Fig. 1F) includes at least a portion of more than one metal protection layer (150a, 150b, para [0028], para [0033]) located on a

portion of the active surface of the semiconductor die, a first passivation layer located on a portion on the metal protection layer, and a plurality of passivation layers (para [0033]) located on at least a portion of the first passivation layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include more than one metal protection layer located on a portion of the active surface of the semicondcuctor die in the invention of Doan since it is well known in the art that multiple metal layers are required in an under bump metallization layer, specifically at least one metal layer is required to be used as an adhesion layer and at least one metal layer is required for a barrier layer.

Moreover, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a plurality of passivation layers located on a portion of a first passivation layer located on a portion of a metal protection layer a die in the invention of Doan since it is desirable to eliminate moisture and static charge build up due to ambient interference.

Regarding claim 37, Doan discloses the limitations of claim 22. Doan does not disclose "wherein the semiconductor die includes a first passivation layer located on a portion thereof and a second passivation layer located on a portion of the first passivation layer." Kuo discloses a semiconductor die (100 of Fig. 1F, for example) which includes a first passivation layer (192c) located on a portion thereof and a second passivation layer (192d) located on a portion of the first passivation layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a second passivation layer located on a portion of a first passivation layer

located on a die in the invention of Doan since it is desirable to eliminate moisture and static charge build up due to ambient interference

Regarding claim 38, Doan discloses the limitations of claim 22, wherein the semiconductor die (Fig. 3A) includes at least a portion of one metal protection layer (146) located on a portion of the active surface of the semiconductor die. Doan does not disclose "a first passivation layer located on a portion of the one metal protection layer, and a second passivation layer located on a portion of the first passivation layer." Kuo discloses a semiconductor die (100 of Fig. 1F) which includes a first passivation (192c) layer located on a portion of the one metal protection layer (150b, para [0028]), and a plurality of passivation layers (para [0033]) located on a portion of the first passivation layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a plurality of passivation layers located on a portion of a first passivation layer located on a metal protection layer located on a die in the invention of Doan since it is desirable to eliminate moisture and static charge build up due to ambient interference.

Regarding claim 39, Doan discloses the limitations of claim 22. Doan does not disclose "wherein the semiconductor die includes at least a portion of more than one metal protection layer located on a portion of the active surface of the semiconductor die, a first passivation layer located on a portion of the more than one metal protection layer, and a plurality of passivation layers located on at least a portion of the first passivation layer." Kuo discloses semiconductor die (100 of Fig. 1F) includes at least a portion of more than one metal protection layer (150a, 150b, para [0028], para [0033])

located on a portion of the active surface of the semiconductor die, a first passivation layer located on a portion on the metal protection layer, and a plurality of passivation layers (para [0033]) located on at least a portion of the first passivation layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include more than one metal protection layer located on a portion of the active surface of the semiconductor die in the invention of Doan since it is well known in the art that multiple metal layers are required in an under bump metallization layer, specifically at least one metal layer is required to be used as an adhesion layer and at least one metal layer is required for a barrier layer.

Moreover, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a plurality of passivation layers located on a portion of a first passivation layer located on a portion of a metal protection layer a die in the invention of Doan since it is desirable to eliminate moisture and static charge build up due to ambient interference.

Regarding claim 45, Doan discloses the limitations of claim 43. Doan does not disclose "further comprising: applying a layer of material to passivate a portion of the area of metal." Kuo discloses applying a layer of material (140) to passivate a portion of an area of metal (138, para [0026]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to passivate a portion of the area of metal in the invention of Doan since it is desirable to have a moisture barrier preventing oxidation of a portion of the area of metal.

Regarding claim 58, Doan discloses the limitations of claim 43. Doan does not disclose "wherein the semiconductor die includes a first passivation layer located on a portion thereof and a second passivation layer located on a portion of the first passivation layer." Kuo discloses a semiconductor die (100 of Fig. 1F) which includes a first passivation layer (192c) located on a portion thereof and a second passivation layer (192d) located on a portion of the first passivation layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a second passivation layer located on a portion of a first passivation layer located on a die in the invention of Doan since it is desirable to eliminate moisture and static charge build up due to ambient interference.

Regarding claim 59, Doan discloses the limitations of claim 43, wherein the semiconductor die (Fig. 3B) includes at least a portion of one metal protection layer (146) located on a portion of an active surface thereof. Doan does not disclose "a first passivation layer located on a portion of the one metal protection layer, and a second passivation layer located on a portion of the first passivation layer." Kuo discloses a semiconductor die (100 of Fig. 1F) which includes a first passivation (192c) layer located on a portion of the one metal protection layer (150b, para [0028]), and a plurality of passivation layers (para [0033]) located on a portion of the first passivation layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a plurality of passivation layers located on a portion of a first passivation layer located on a metal protection layer located on a die in the invention of

Doan since it is desirable to eliminate moisture and static charge build up due to ambient interference.

Regarding claim 60, Doan discloses the method of claim 43. Doan does not disclose "wherein the semiconductor die includes at least a portion of more than one metal protection layer located on a portion of an active surface thereof, a first passivation layer located on a portion of the more than one metal protection layer, and a plurality of passivation layers located on at least a portion of the first passivation layer." Kuo discloses semiconductor die (100 of Fig. 1F) includes at least a portion of more than one metal protection layer (150a, 150b, para [0028], para [0033]) located on a portion of the active surface of the semiconductor die, a first passivation layer located on a portion on the metal protection layer, and a plurality of passivation layers (para [0033]) located on at least a portion of the first passivation layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include more than one metal protection layer located on a portion of the active surface of the semiconductor die in the invention of Doan since it is well known in the art that multiple metal layers are required in an under bump metallization layer, specifically at least one metal layer is required to be used as an adhesion layer and at least one metal layer is required for a barrier layer.

Moreover, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a plurality of passivation layers located on a portion of a first passivation layer located on a portion of a metal protection layer a die in the

invention of Doan since it is desirable to eliminate moisture and static charge build up due to ambient interference.

Regarding claim 79, Doan discloses the limitations of claim 64. Doan does not disclose "wherein the semiconductor die includes a first passivation layer located on a portion thereof and a second passivation layer located on a portion of the first passivation layer." Kuo discloses a semiconductor die (100 of Fig. 1F) which includes a first passivation layer (192c) located on a portion thereof and a second passivation layer (192d) located on a portion of the first passivation layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a second passivation layer located on a portion of a first passivation layer located on a die in the invention of Doan since it is desirable to eliminate moisture and electrical static charge build up due to ambient interference.

Regarding claim 80, Doan discloses the limitations of claim 64, wherein the semiconductor die (Fig. 3B) includes at least a portion of one metal protection layer (146) located on a portion of the active surface thereof. Doan does not disclose "a first passivation layer located on a portion of the one metal protection layer, and a second passivation layer located on a portion of the first passivation layer."

Kuo discloses a semiconductor die (100 of Fig. 1F) which includes a first passivation (192c) layer located on a portion of the one metal protection layer (150b, para [0028]), and a plurality of passivation layers (para [0033]) located on a portion of the first passivation layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a plurality of passivation layers located on a

portion of a first passivation layer located on a metal protection layer located on a die in the invention of Doan since it is desirable to eliminate moisture and static charge build up due to ambient interference.

Regarding claim 81, Doan discloses the limitations of claim 64. Doan does not disclose "wherein the semiconductor die includes at least a portion of more than one metal protection layer located on a portion of the active surface thereof, a first passivation layer located on a portion of the more than one metal protection layer, and a plurality of passivation layers located on at least a portion of the first passivation layer."

Kuo discloses semiconductor die (100 of Fig. 1F) includes at least a portion of more than one metal protection layer (150a, 150b, para [0028], para [0033]) located on a portion of the active surface of the semiconductor die, a first passivation layer located on a portion on the metal protection layer, and a plurality of passivation layers (para [0033]) located on at least a portion of the first passivation layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include more than one metal protection layer located on a portion of the active surface of the semiconductor die in the invention of Doan since it is well known in the art that multiple metal layers are required in an under bump metallization layer, specifically at least one metal layer is required to be used as an adhesion layer and at least one metal layer is required for a barrier layer.

Moreover, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a plurality of passivation layers located on a portion of a first passivation layer located on a portion of a metal protection layer a die in the

invention of Doan since it is desirable to eliminate moisture and static charge build up due to ambient interference.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer Matisiak whose telephone number is 571-272-2639. The examiner can normally be reached on Business Days 9:30a-6:30p EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 517-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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